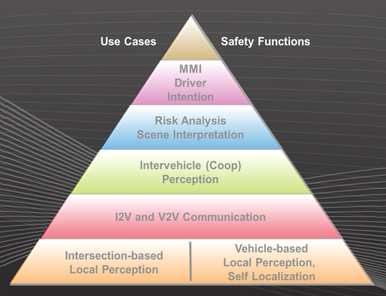
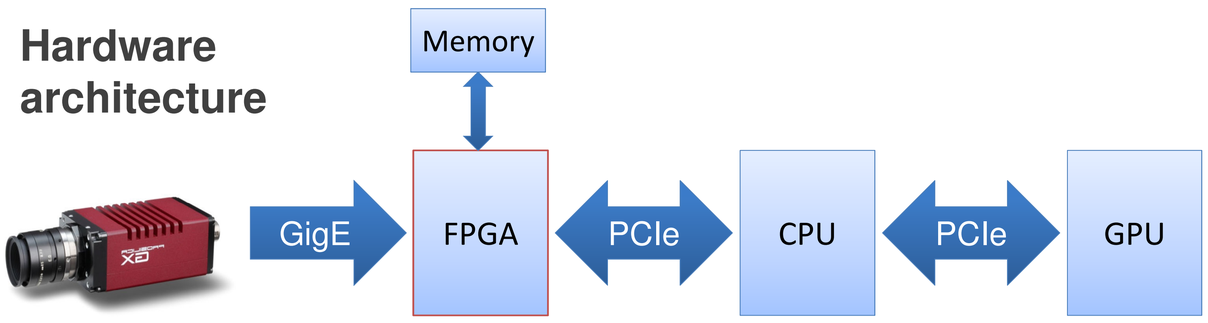


Real-Time Pedestrian Recognition via FPGA-Powered High-Resolution Image Sequence Processing

Project Ko-PER

FORSCHUNGSINITIATIVE
K O - F A S

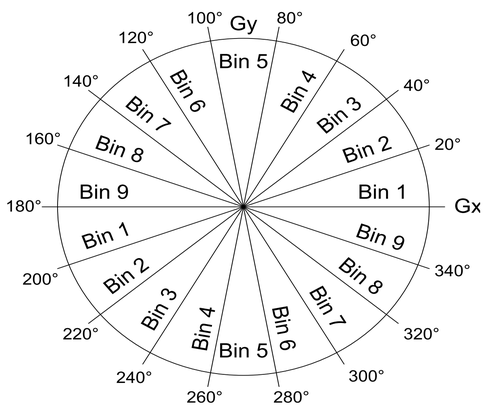
Hardware architecture

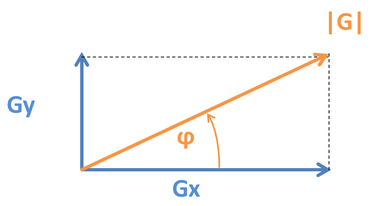


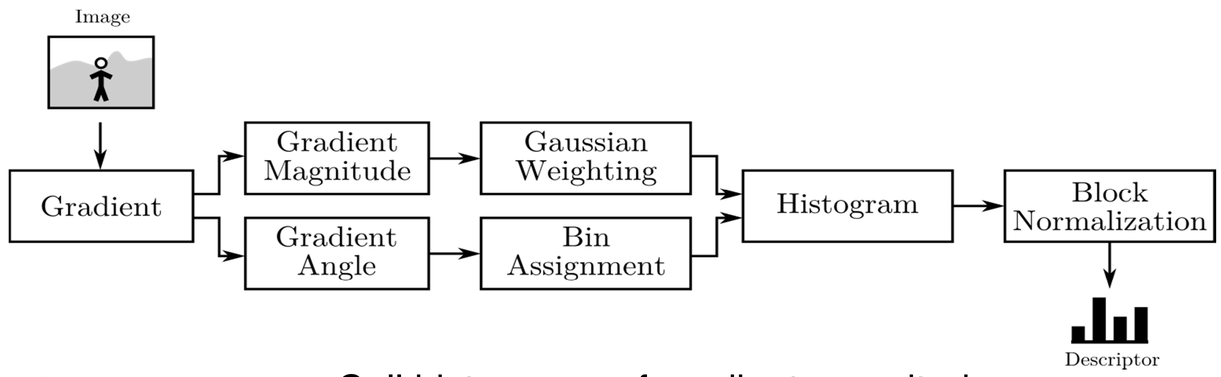
Requirements

- Resolution: 1920 x 1080 pixels (Full-HD)
- Frame rate: min. 50 fps
- Multi-scale: 15 – 20 scales

HOG-Descriptor







- Global *Descriptor* with 3780 elements
- Based on gradients
- Divide orientation into 9 bins

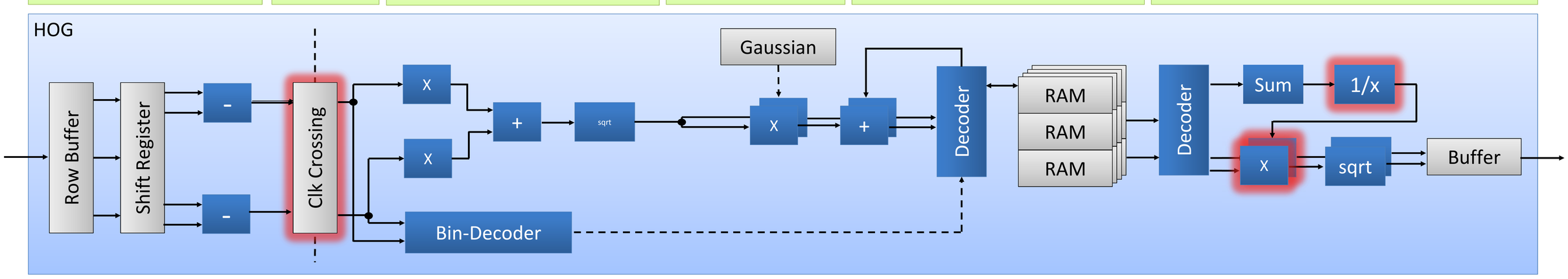
- Cell histograms of gradient magnitudes
- Concatenate histogram result in HOG descriptor

Implementation

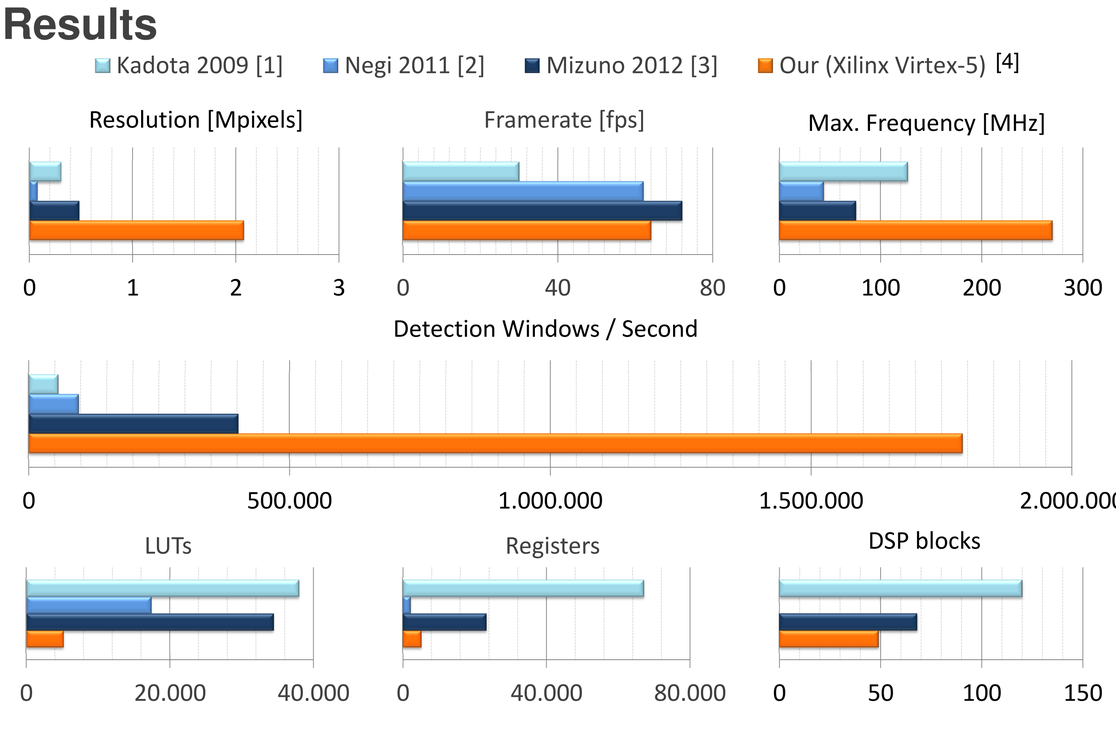
$$\overrightarrow{x_B} \rightarrow \sqrt{\frac{\overrightarrow{x_B}}{\sum_i x_{B_i} + \varepsilon}} \quad \Rightarrow \quad \overrightarrow{x_B} \rightarrow \sqrt{\overrightarrow{x_B} \cdot \frac{1}{\sum_i x_{B_i} + \varepsilon}}$$

- Serialization of calculations by clock doubling saves resources
- High resource reduction by serializing the normalization

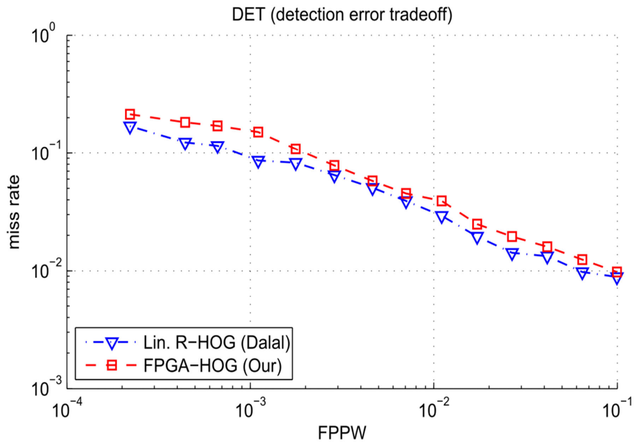
Derivation	Core Clock	Gradient Magnitude & Bin Assignment	Gaussian Weighting	Cell Histogram Creation	Block Histogram Creation & Normalizing



Results



- Cell-based approach for storage reduction and throughput increase
- High resource reduction by clock doubling (serialization)
- Calculation of multiple scales in parallel
- Time-Multiplex to increase number of scales beyond resource limitations
- Good detection rate despite simplification of the algorithm



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