Project Ko-TAG

System Architecture

FORSCHUNGSINITIATIVE
K O - F A S

Design of the Ko-TAG devices

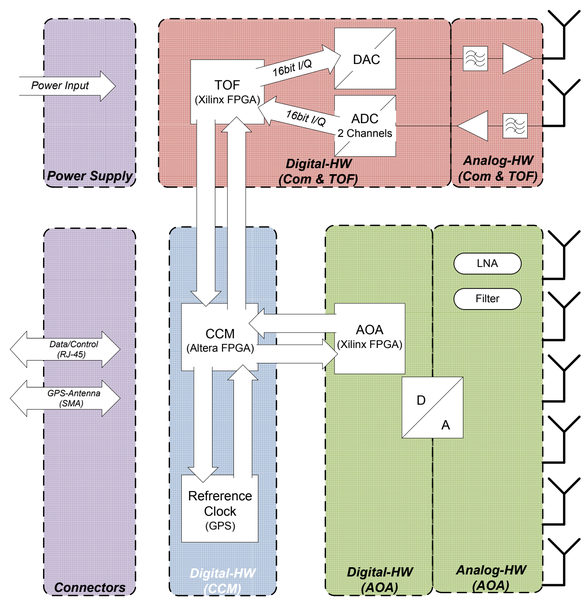
Localization Unit (LU)

TOF Components [TUM]

- digital hardware implemented in a Xilinx Spartan FPGA
- relative distance measurements to remote objects using Time of Flight (TOF) method
- analog radio frontend used for communication and TOF measurements

AOA Components [IIS]

- digital hardware implemented in a Xilinx Spartan FPGA and an Analog Devices DSP
- Angle of Arrival (AOA) Measurements
- analog radio frontend with an 2D antenna array used for AOA measurements



Communication & Control Module (CCM) [sizedn]

- Network Communication & Management (incl. security, privacy, address management …)
- implemented on an Altera ArriaIIGX FPGA
- control and coordination of TOF and AOA sub modules
- external reference clock for synchronization of spatially distributed OBUs
- communication to the Fusion Unit (FU) via Ethernet and LocON protocols

SafeTAG (ST)

TOF Components [TUM]

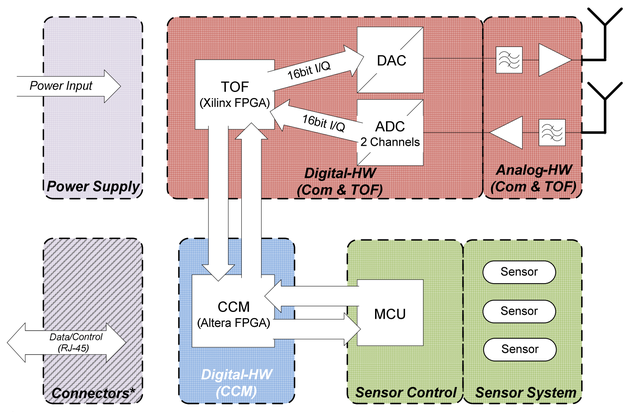
- digital hardware implemented in a Xilinx Spartan FPGA
- reply to TOF requests at the specified time slot
- analog radio frontend used for communication and TOF measurements

Sensor Control [IIS]

- access to several local sensors
- communication with the CCM via a serial Interface and a reduced LocON protocol
- determination of movement patterns

Communication & Control Module (CCM) [sizedn]

- Network Communication & Management (incl. security, privacy, address management …)
- implemented on an Altera ArriaIIGX FPGA
- control and coordination of sensor



*only present for omnidirectional safety

Communication & Control Module

The system design used for the Ko-TAG project allows easy exchange or extension of given devices. The Communication Control Module (CCM) has a modular structure as well.

Both hardware and firmware are based on the same modules for all the devices types and can be built up as required. Localization Units (LUs), SafeTAGs (STs) and VehicleTAGs (VTs) can be configured on the same CCM (Communication & Control Module) hardware using different FPGA and Firmware images.

NIOS II Soft-core Dual-Core CPU

- network management
- coordination and control of the single IP-Cores and external sub modules (e.g. TOF, AOA)

IEEE 802.11p digital PHY (dPHY) [HHI]

- baseband modulation conforming to IEEE802.11p standard for Car2Car communication

Data Chain

- interconnects CPU (Firmware) and dPHY
- CRC generation/validation
- address validation
- en-/decryption of data frames

Timer/Synchronization

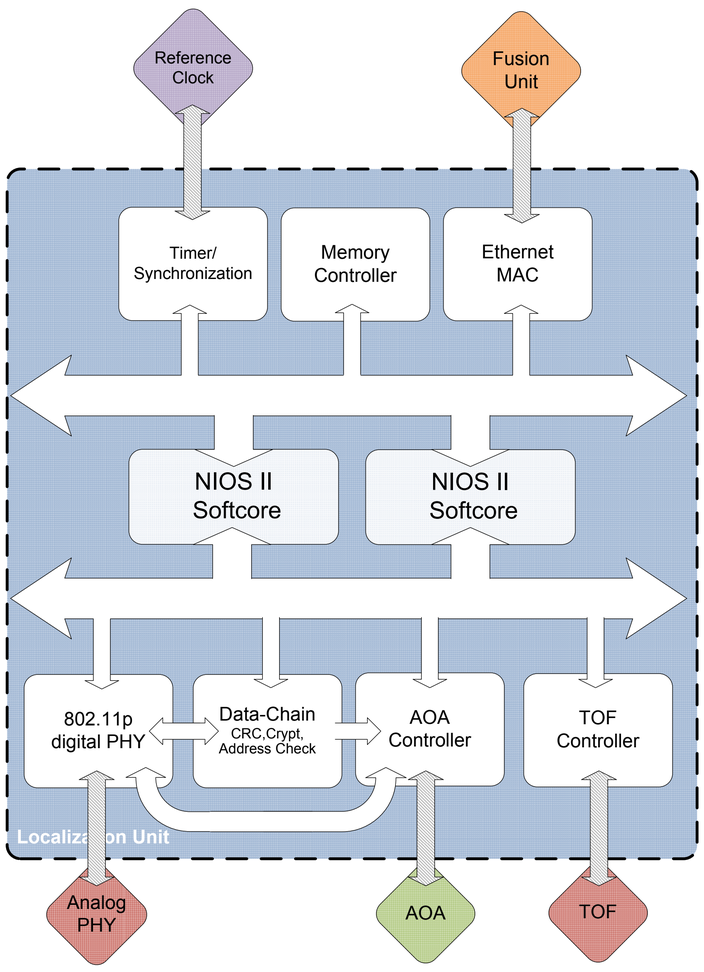
- synchronization of spatially distributed OBUs via external Reference Clock (e.g. GPS)
- provision of timers/counters in synchronized mode

Gigabit Ethernet MAC

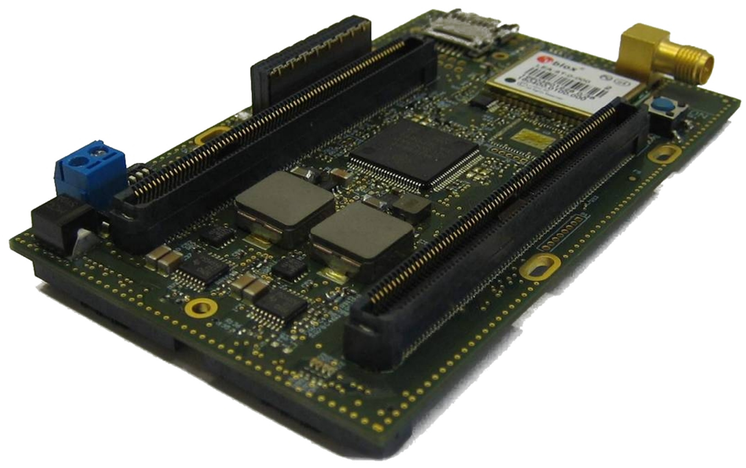
- interconnect to FU
- debug and monitoring interface during development & integration process

TOF Controller

AOA Controller



	Localization Unit	SafeTAG	RUS-TAG
802.3 MAC	X		X
Time Reference	X		
AOA-Interface	X		
INS-Interface		X	
TOF-Interface	X	X	X



BMW Group Forschung und Technik
DAIMLER
Fraunhofer Heinrich-Hertz-Institut
Technische Universität München
Continental
Fraunhofer IIS
Steinbeis-Innovationszentrum Embedded Design und Networking
Supported by:
Federal Ministry of Economics and Technology
on the basis of a decision by the German Bundestag